UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/692,110	10/23/2003	Mohan R. Nagar	01-179	6569

7590 02/09/2005

LSI Logic Corporation
Legal Department-IP
MS D-106
1621 Barber Lane
Milpitas, CA 95035

EXAMINER	
CHAN, EMILY Y	

ART UNIT	PAPER NUMBER
2829	

DATE MAILED: 02/09/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/692,110	NAGAR ET AL.	
	Examiner	Art Unit	
	Emily Y. Chan	2829	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 October 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4 and 9-15* is/are pending in the application.

4a) Of the above claim(s) *5-8* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4 and 9-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *23 October 2003* is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Restriction to one of the following inventions is required under 35 U.S.C. 121:

I. Claims 1-4 and 9-15, drawn to a probe card and a method for measuring package interconnect impedance, classified in class 324, and subclass 754.

II. Claims 5-8, drawn to a method of making a probe card, classified in class 29, subclass 830.

The inventions are distinct, each from the other because:

Inventions I and II are related as product and process of making. The inventions are distinct if either or both of the following can be shown: (1) that the process as claimed can be used to make other and materially different product or (2) that the product as claimed can be made by another and materially different process (MPEP § 806.05(f)). In the instant case the product as claimed can be made by another and materially different process such as a chemical etching process as shown by US Patent Number 5, 060,371.

During a telephone conversation with Mr. Henry J. Groth on 2-2-05 a provisional election was made without traverse to prosecute the invention of I, claims 1-4 and 9-15. Affirmation of this election must be made by applicant in replying to this Office action. Claims 5-8 are withdrawn from further consideration by the examiner, 37 CFR 1.142(b), as being drawn to a non-elected invention.

Drawings

The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the following reference sign(s) mentioned in the description: reference No. 40 is not shown in Fig. 2. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the claimed **connected between the DUT/load board (16) and the tester (12)** recited in claim 9 must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

2. Claims 4, 9 and 13 are s rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

In the instant application, for claim 4, the claimed "a first alloy disposed on a second alloy" is not described in the specification and shown in drawings and for claims 9 and 13, the claimed " interconnect impedance versus time data" is critical or essential to the practice of the invention but is not explained in detail in the specification. In the specification, page, 9, lines 15-16, it only mentions that the post processing software 34 is used to obtain the "interconnect impedance versus time for the device (i.e., package) under test, however, it fails to explain where the time data come from and how the interconnect impedance versus time data is generated.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 9 and 13 are rejected under 35 U.S.C. 112, second paragraph, as failing to set forth the subject matter which applicant(s) regard as their invention.
The recitation that " provide interconnect impedance versus time data" is unclear because it is not specified where the time data come from originally and that the "interconnect impedance" is result of the interconnection of the first surface or the interconnection of the second surface of the probe card.

Claim Objections

Claim 13 is objected to because of the following informalities:

On line 6, "the substrate" lacks antecedent basis. Appropriate correction is required.

Claim Rejections - 35 USC § 102

(a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

4. Claims 1 and 3-4 are rejected under 35 U.S.C. 102(a) as being anticipated by Nagar US Patent No. 6,605,954.

With respect to claim 1, Nagar ('954) discloses a probe card (see Fig. 1) mountable to a device under test (DUT) board tester (see Col. 3, line, 55 "test station") as claimed, comprising: a substrate (26) having a solder balls (2) on one side and solder on pad (SOP) (4) on the other side; probe pins (6) in contact with the SOP (4), the probe pins (6) being connected to the substrate (26) via the SOP (4) and being engageable with the solder pumps (8) on a wafer (12).

With respect to claims 2-3, Nagar ('954) discloses that the substrate (26) is preferably an electrically non conducting substrate (see Col. 2, line 43-44) which meets the claimed the substrate is organic for claim 2, and is ceramic for claim 3 because it is well known that the organic and ceramic material are not conductive.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nagar ('954).

Nagar ('954) fails to disclose that his SOP (4) comprising the different alloys; however, since it is well known that the use of the alloy material (i.e., conductive material) for electrical contacting and Nagar ('954) does not specify the requirement of using the same alloys for his SOP (4). Therefore, the use the different alloys to build up the SOP as claimed in Nagar ('954) would have been within the level of ordinary skill in the art.

6. Claims 9-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Swart US Patent No. 6,191,601 in view of DiOrio et al US Publication, 2004/0217767.

Swart ('601) expressly discloses a method and a test fixture for measuring impedance (see Figs 1-4) as claimed, comprising: a tester (20), a device under test (DUT)/load board (16) which is configured to retain a substrate, (see Col.3, lines 61-62), the tester (20) being connected to a Digital Sampling Oscilloscope)(TDR 46) configured to receive a reflected signal (the matched impedance test signals) from the substrate (see Fig. 2 and Col. 5, lines 5-8) and provide the reflected signal (the matched impedance test signals) to the tester (see Fig. 2 and Col. 5, lines 10-12) which is configured to analyze the reflected signal.

Swart ('601) does not specify that : (1) his tester (20) providing " interconnect impedance versus time data" and (2) a probe card comprising solder balls on a first

surface and an electrically conductive material on a second surface that is configured to electrically contact bumps on the substrate.

As to (1) above, since applicant does not explain "what the "interconnect impedance versus time data" is (see rejection above) and since Swart ('601) 's tester (20) has the same circuit connection structure as claimed, it would have been obvious to one of ordinary skill in the art that Swart ('601) 's tester (20) can provide " the interconnect impedance versus time data" as claimed.

As to (2) above, DiOrio et al ('767) disclose wafer probing and particularly teach probe (see Fig 2, interconnect substrate 220 and Fig. 3 probe card 330) comprising solder balls (222) on a first surface and an electrically conductive material on a second surface (340) that is configured to electrically contact bumps (112) on a substrate (350).

It would have been obvious to one of ordinary skill in the art at the time the claimed invention was made to incorporate the probe card of DiOrio et al ('767) into Swart ('601)'s system because DiOrio et al ('767) discloses that his probe card provides durable alignment for testing of integrated circuits (see page 1, paragraph (0010) last 7 lines).

With respect to claims 10 and 14, DiOrio et al ('767) discloses his solder balls (222) mountable to a test head inter phase board (320) of the tester (310).

With respect to claims 11 and 15, DiOrio et al ('767) discloses that his probe card (330, 340) does not have any probe pins.

With respect to claim 12, DiOrio et al ('767) discloses that his probe card (330, 340) is configured to make electrical contact with pumps (112) on the substrate (350) without using probe pins.

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Hilton ('482) disclose ball grid array package (see Figs 4-5) and particularly teach a ball grid array adapter (20) or a probe card comprising solder balls (24) on a first surface (25) and a second surface (29) that is configured to electrically contact bumps (30) on the substrate (31).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Emily Y. Chan whose telephone number is 571-272-1956. The examiner can normally be reached on 8:30-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nestor Ramirez can be reached on 571-272-2034. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

EC
2-3-05

VINH NGUYEN
PRIMARY EXAMINER
A.U. 2829
02/06/05